**axis\_readout\_v3**

Introduction

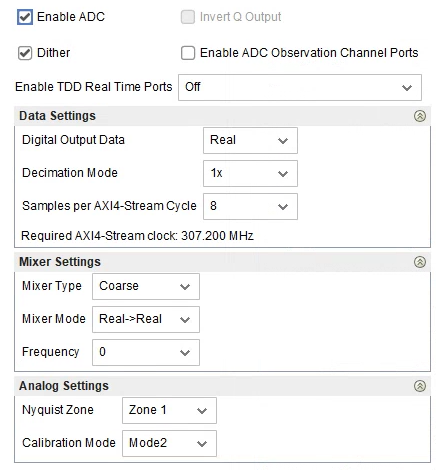
Compare to axis\_pfb\_readout\_v2, this can only demodulate a frequency at a time, but the max frequency it can demodulate could be much higher than that of axis\_pfb\_readout\_v2 limited only by the max sampling rate of ADC.

how to include it in firmware (zcu216, vivado2020.2)

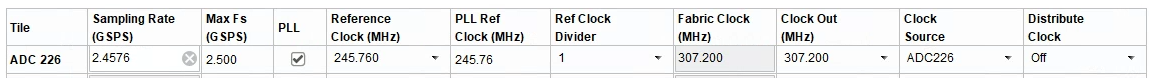
IP core settings (double click on the ip):

* “Fullspeed Output” checked

RFDC (Zynq Ultrascale+ RF Data Converter) DAC settings:



RFDC ADC tile clocking settings:



Wirings:

* The ”Clock converter” below is needed only if the clock speed of muxed sg (aclk) is different from that of tproc (aclk).
* For full details, you can re-create the vivado block design using the scripts (bd\_216 … .tcl, proj\_216 … .tcl) at:

<https://github.com/Ri-chard-Wu/thesis/tree/master/codes/axis_sg_mux4_v2-test-216>

If you don’t know how to use the scripts, see the section *export & re-create vivado block design*.

