**axis\_readout\_v2**

Introduction

Compare to axis\_pfb\_readout\_v2, this ip can only demodulate a frequency at a time, but the max frequency it can demodulate could be much higher than that of axis\_pfb\_readout\_v2 limited only by the max sampling rate of ADC.

Specs

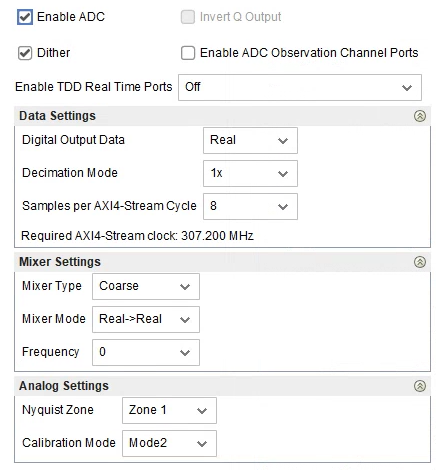
* Frequency (fs is sampling rate of ADC): max input frequency is fs; min input frequencies may be limited by external RF circuits (e.g. baluns).

How to include it in firmware (zcu216, vivado2020.2)

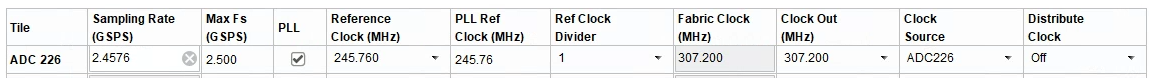
IP core settings (double click on the ip):

* “Fullspeed Output” checked

RFDC (Zynq Ultrascale+ RF Data Converter) DAC settings:



RFDC ADC tile clocking settings:



Wirings:

* For full details, you can re-create the vivado block design using the scripts (bd\_216 … .tcl, proj\_216 … .tcl) at:

<https://github.com/Ri-chard-Wu/thesis/tree/master/codes/full-speed-ro-sg-bd-scripts-216>

If you don’t know how to use the scripts, see the section *export & re-create vivado block design*.

